Case Study: SerDes, HSIO & Thermal Sensor – Design/Layout

16G SerDes Design & Layout

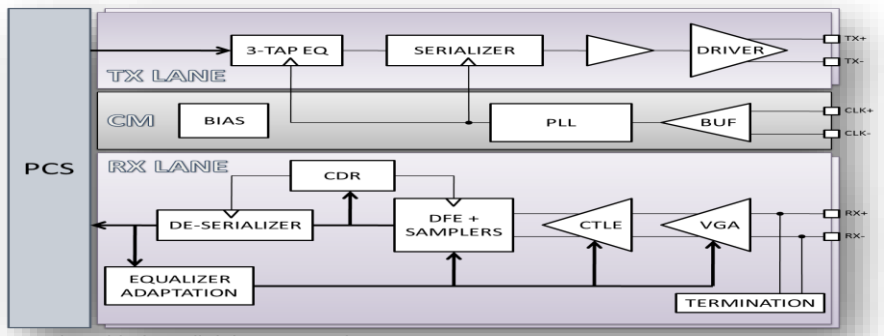
The 16GHz Serdes was designed in 16nm process. Team was Involved in circuit design and Layout of both TX & RX.

Responsibility :

- Circuit Design of TX -Equalizer, Sampler, De-serializer, DFE ,CTLE & PLL.
- Floorplan of complete TX & RX layout delivery from scratch.
- Buffer design for output of clock channels going to Final driver.
- Context dependency layout to take care of coupling, matchings EM etc.
- ESD related checks for Clamp diodes.

Tools used : Cadence tool suite, Caliber (Mentor) & Hspice

Engagement Model : A team of 10 Engineers for 1 year onsite/offsite mixed



HSIO

- UXPHY3.1 supporting 28.1Gbps SERDES, 7nm process
- Design support included various TX, RX and Common Lane blocks.
- Complete post layout simulation with Specifications were met. All other collaterals like RV, Aging, EOS, ERC, Timing were covered to ensure good quality.
- Design and verification expertise in High-speed Drivers, Parallel to serial converters, DFE, squelch, LDO, RCOMP blocks.

Duration: 12 months

Engagement Model: T&M, 10 Engineers

Digital Thermal Sensor

- DTS Nx Gen1, CKT Sim, Polo sims, 5nm process
- Functional & Performance Val
- Reliability Sim (Aging, Early life Failure (ELF), Electrical over Stress (EOS), RV)
- Mixed signal Verification (MSV)

Duration: 11 months

Engagement Model: T&M, 4 Engineers